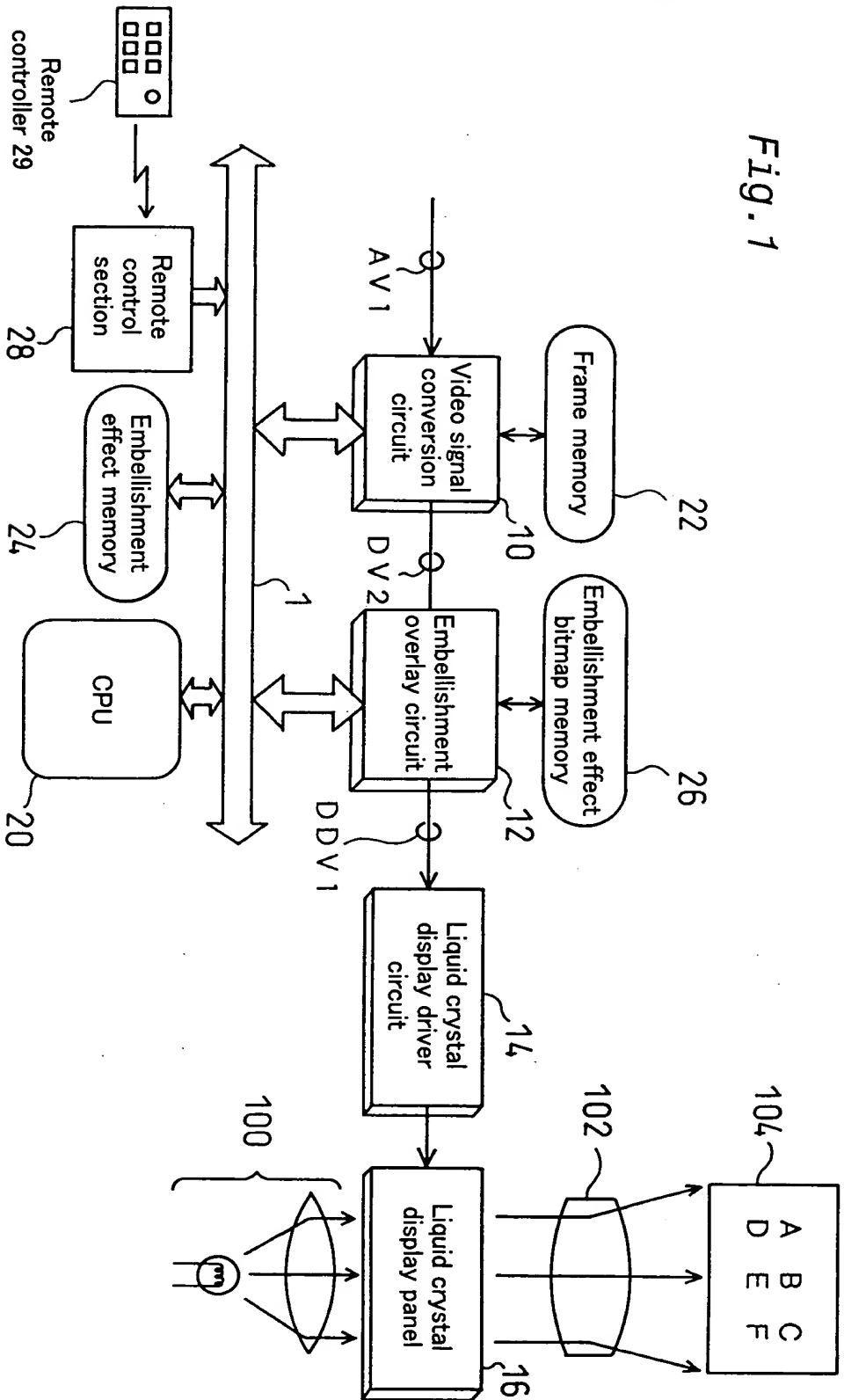


Fig. 1



Block diagram of a video processing system 10. The system includes a Frame memory (22) connected to a Video processor (34). The Video processor (34) is connected to an A-D conversion section (32). The A-D conversion section (32) is connected to a Sync separator (30). The Sync separator (30) outputs RGB signal S1 and Composite image signal S2. The Sync separator (30) also receives Color signal S3. The A-D conversion section (32) receives DV1 and outputs DV2. The Video processor (34) receives DCLK and WSYNC and outputs RSYNC. The system is powered by AV1.

Fig. 3 (a)

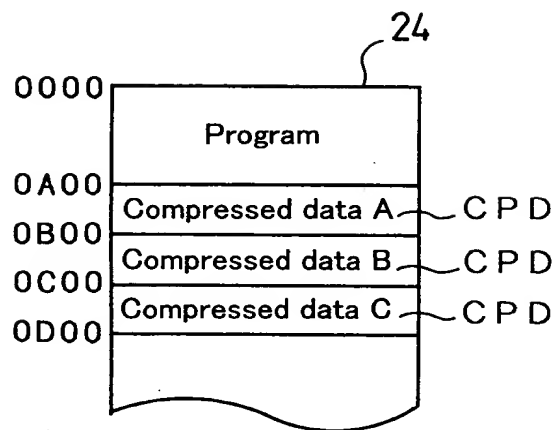


Fig. 3 (b)

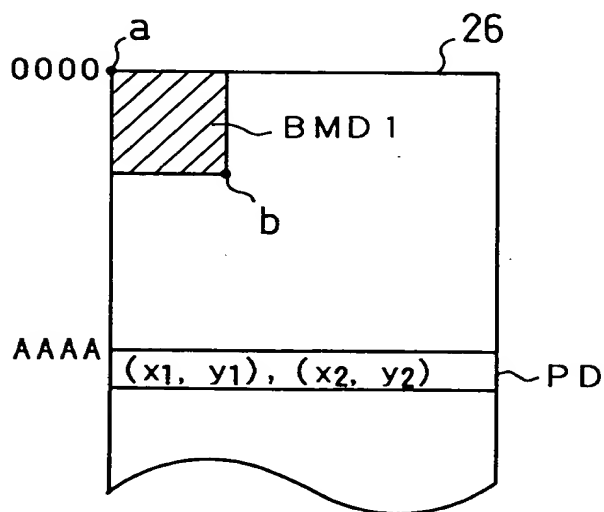


Fig. 3 (c)

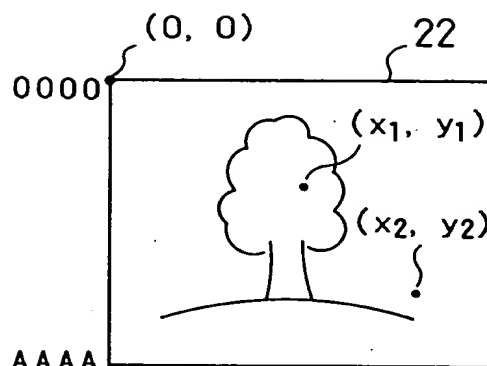


Fig. 4

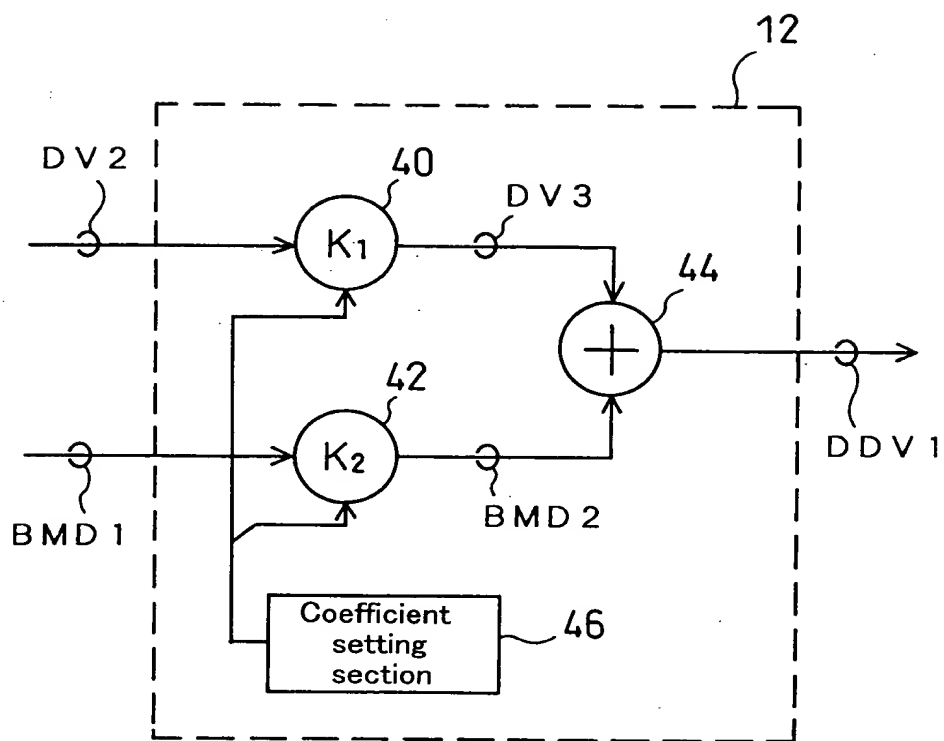


Fig. 5 (a)

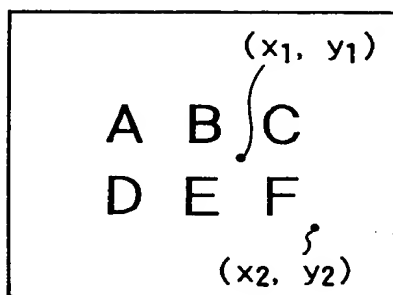


Fig. 5 (c)

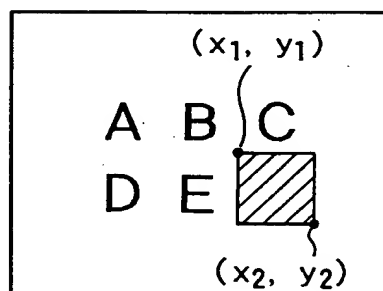


Fig. 5 (b)

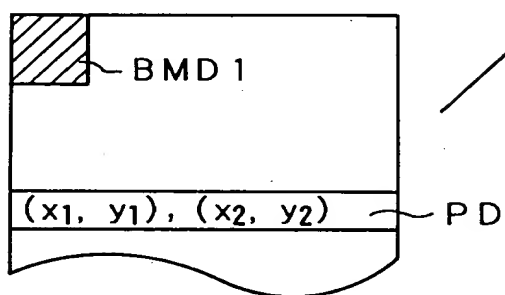


Fig. 6

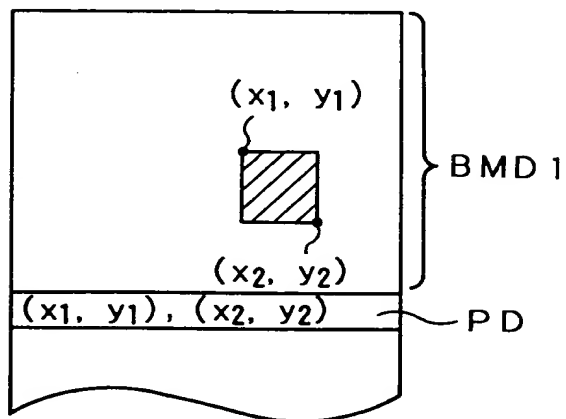


Fig. 7 (a)

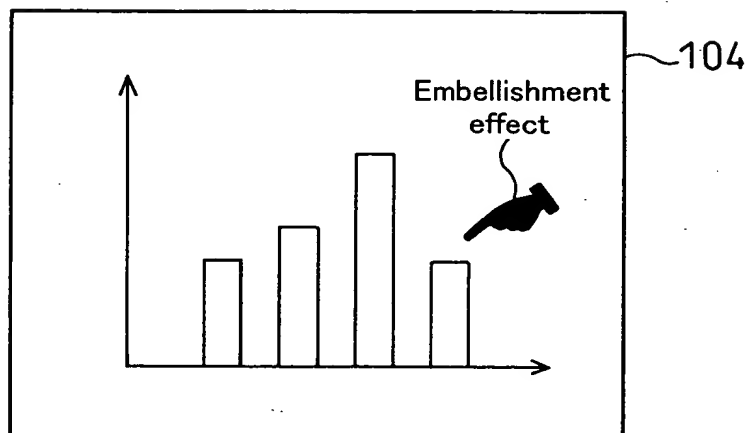


Fig. 7 (b)

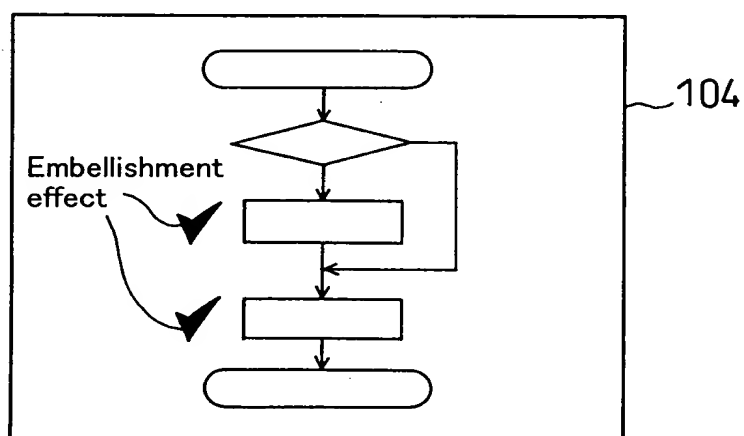


Fig. 7 (c)

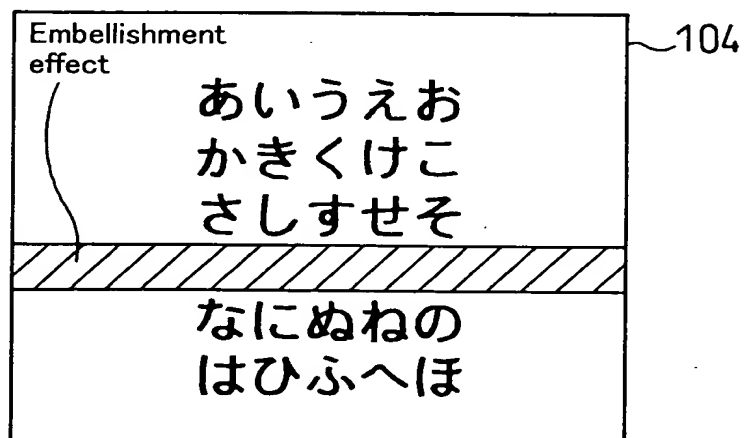


Fig. 8 (a)

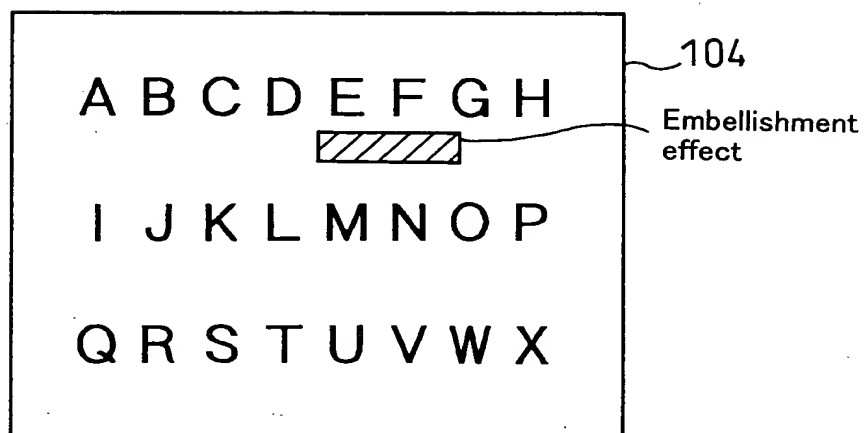


Fig. 8 (b)

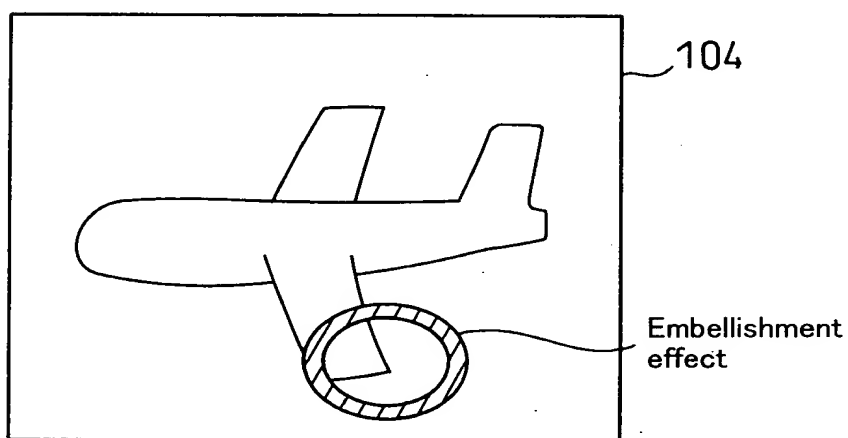


Fig. 8 (c)

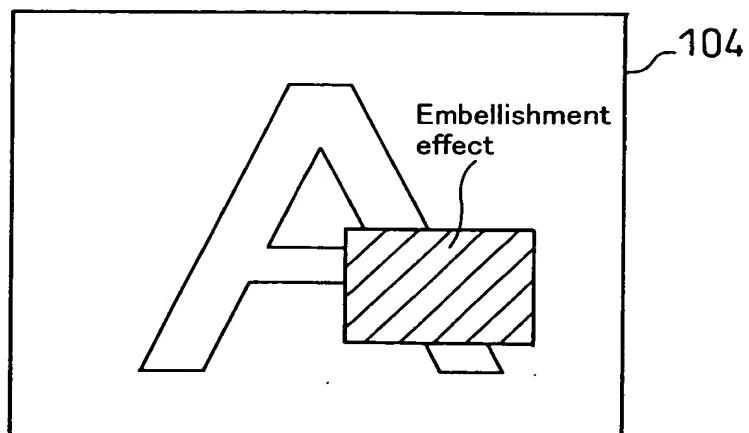


Fig.9

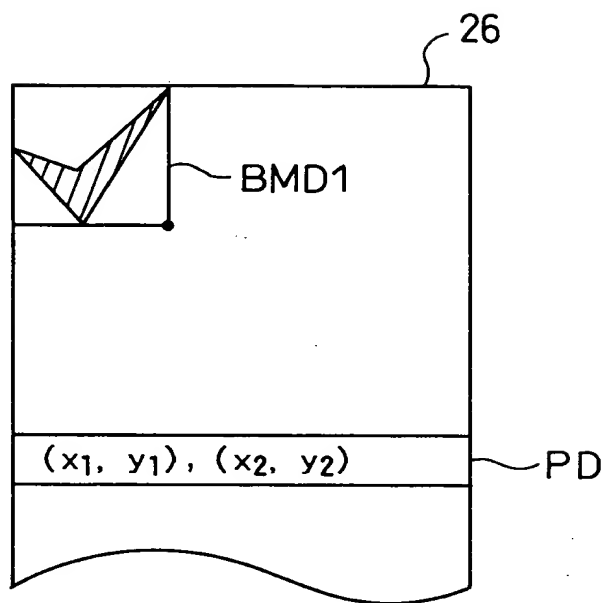


Fig. 10 (a)

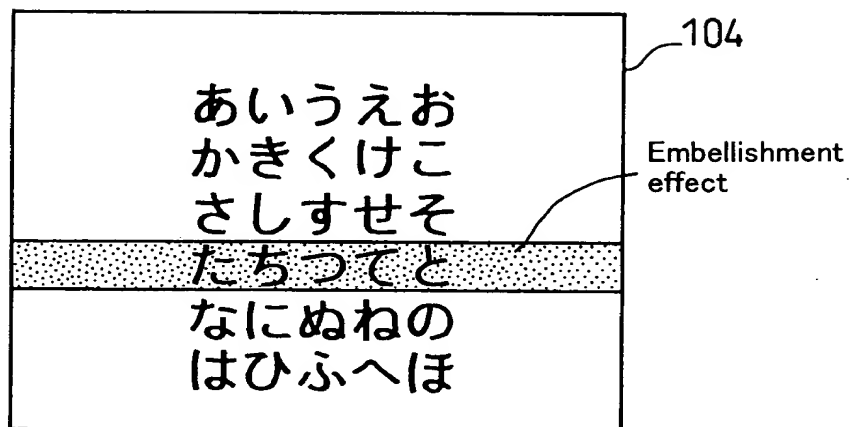


Fig. 10 (b)

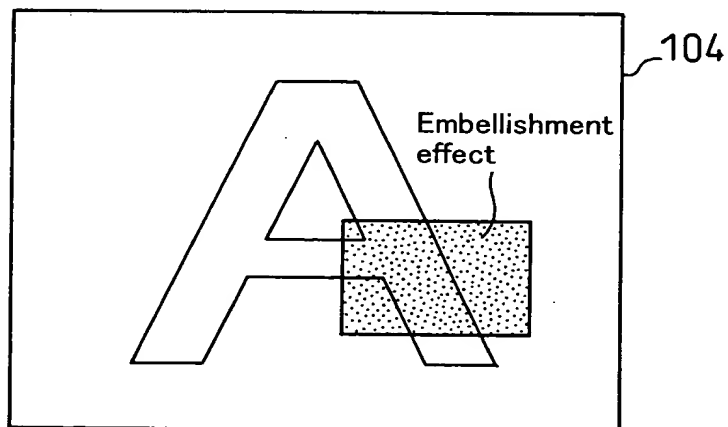


Fig. 11(a)

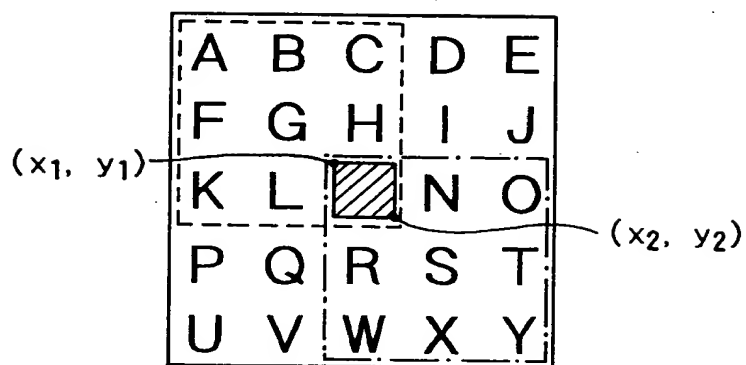


Fig. 11(b)

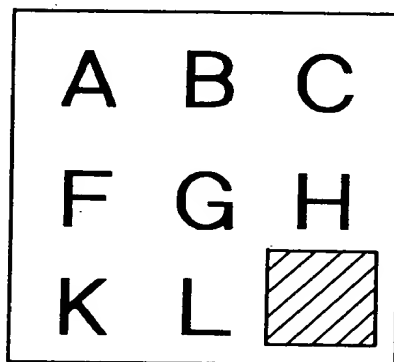


Fig. 11(c)

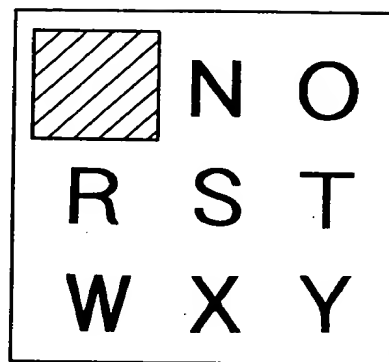


Fig. 14

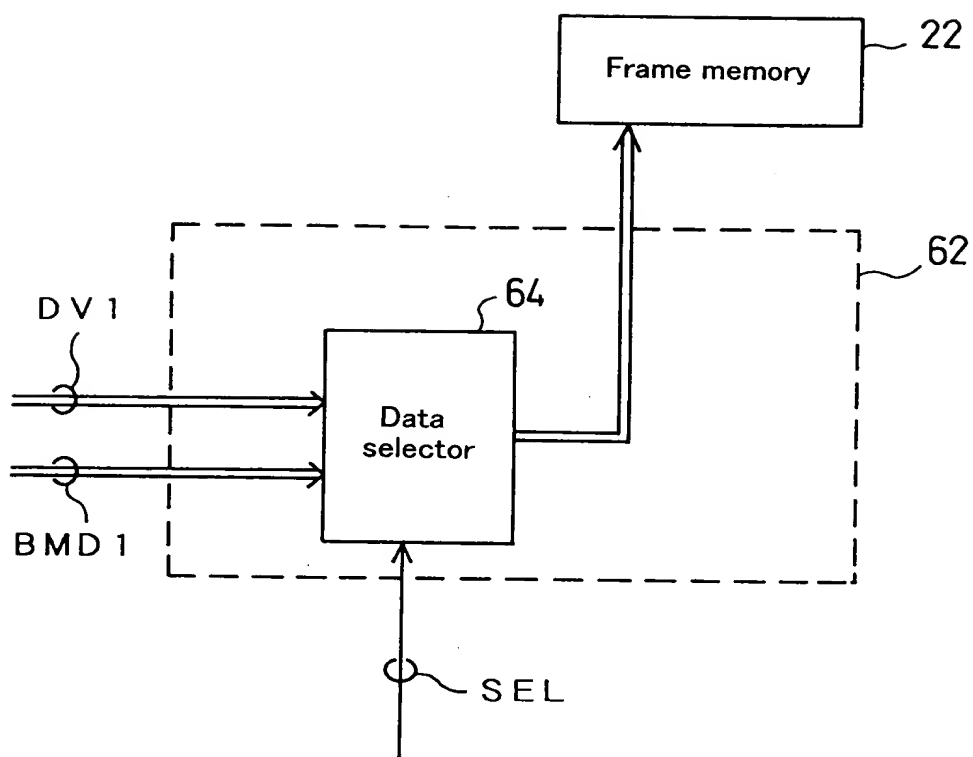




Fig. 16

Block diagram of a video processing system (Fig. 16). The system is enclosed in a dashed box 210. It includes a "Sync separator" block 230, an "A-D conversion section" block 232, a "video processor" block 234, and "Frame memory" block 222. Inputs to the system are "RGB signal S1", "Composite image signal S2", "A V 1", "DCL K", "WSYNC", and "R SYNC". The "Sync separator" 230 outputs "Color signal S3" to the "A-D conversion section" 232. The "A-D conversion section" 232 outputs "D V 1" to the "video processor" 234. The "video processor" 234 outputs "D V 2" and is connected to "Frame memory" 222 via a bidirectional arrow. The "video processor" 234 also receives "DCL K" and "WSYNC" signals. The "R SYNC" signal is also an input to the system.

Fig. 18 (a)

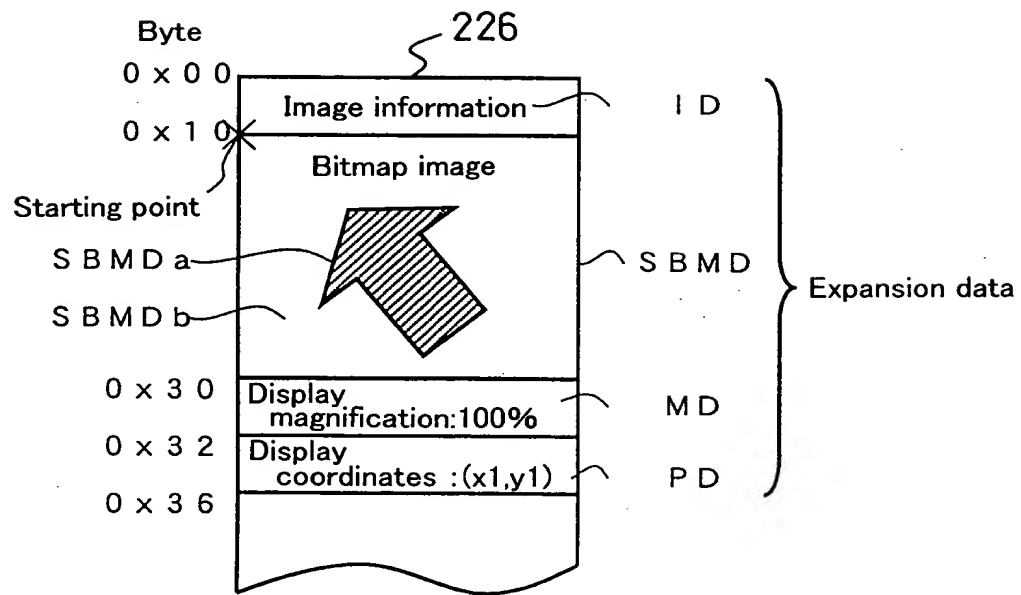


Fig. 18 (b)

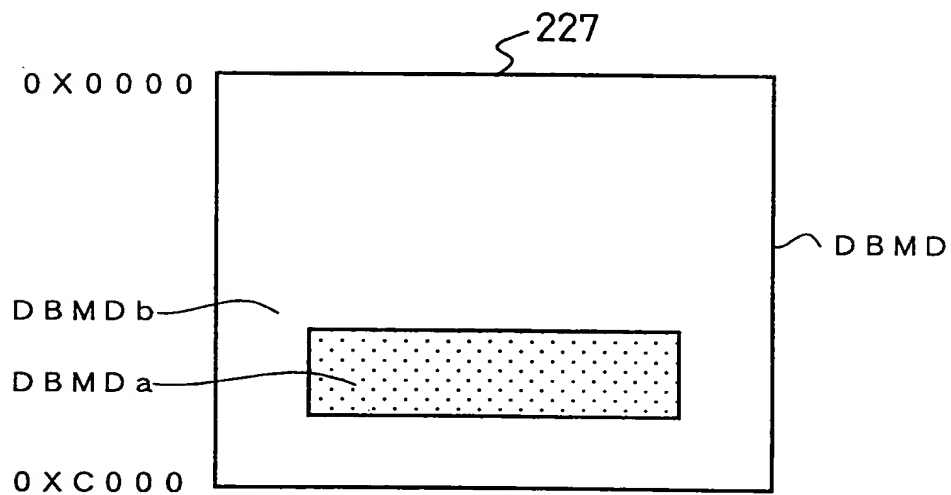
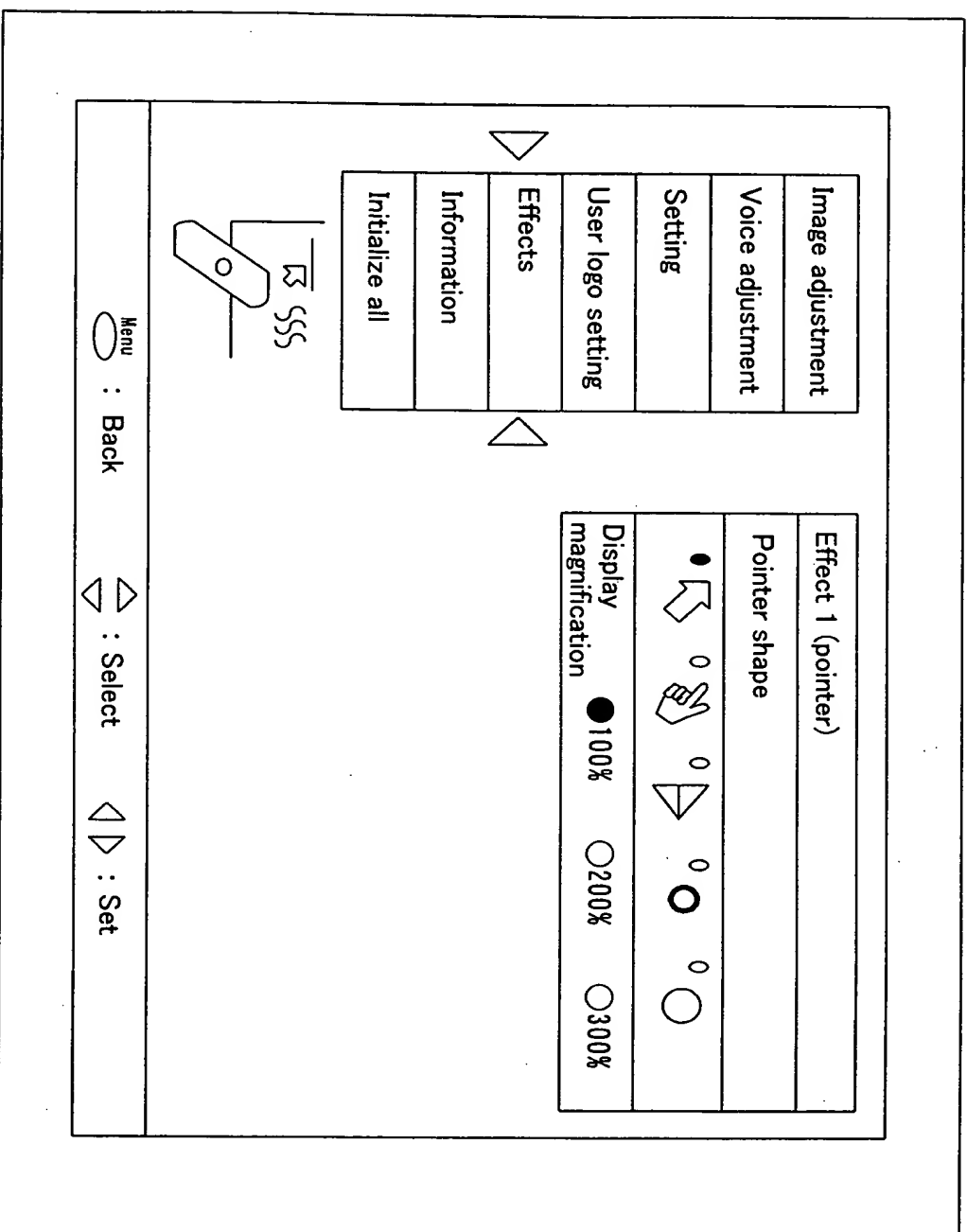


Fig. 19



104

Fig. 20(a)

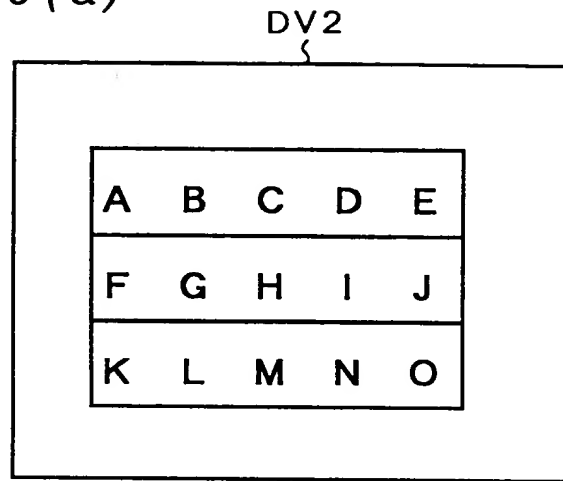


Fig. 20(b)

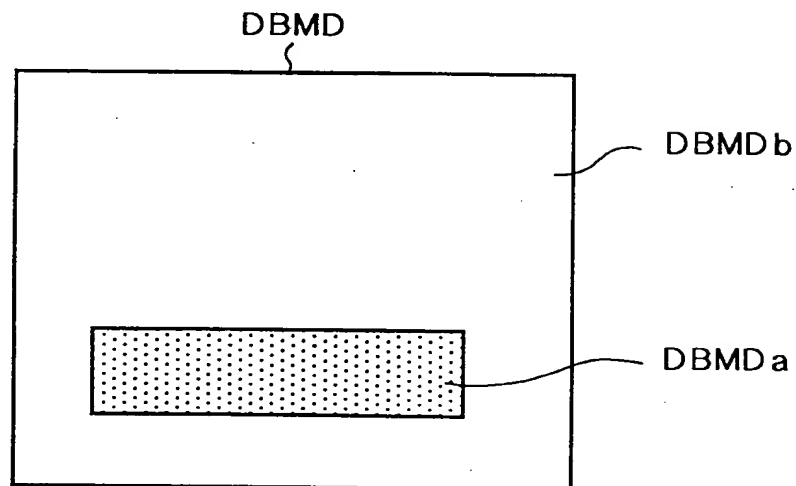


Fig. 20(c)

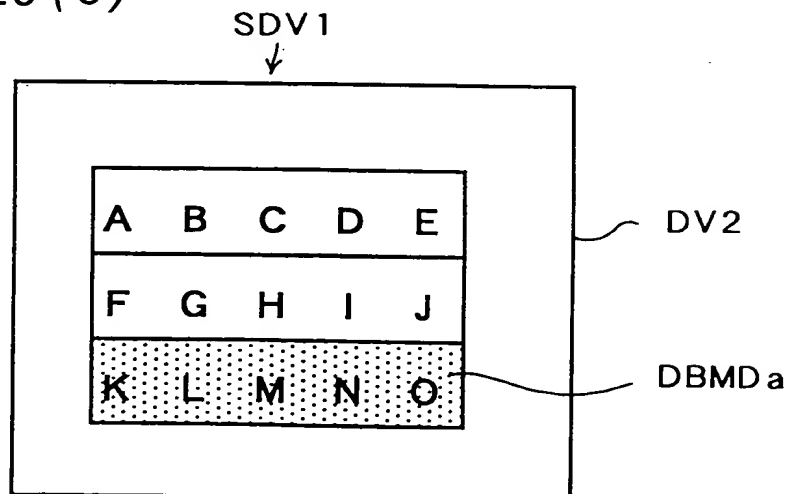


Fig.21(a)

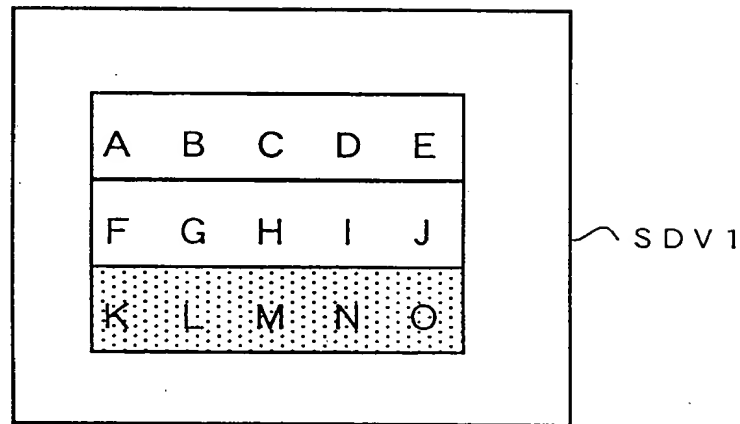


Fig.21(b)

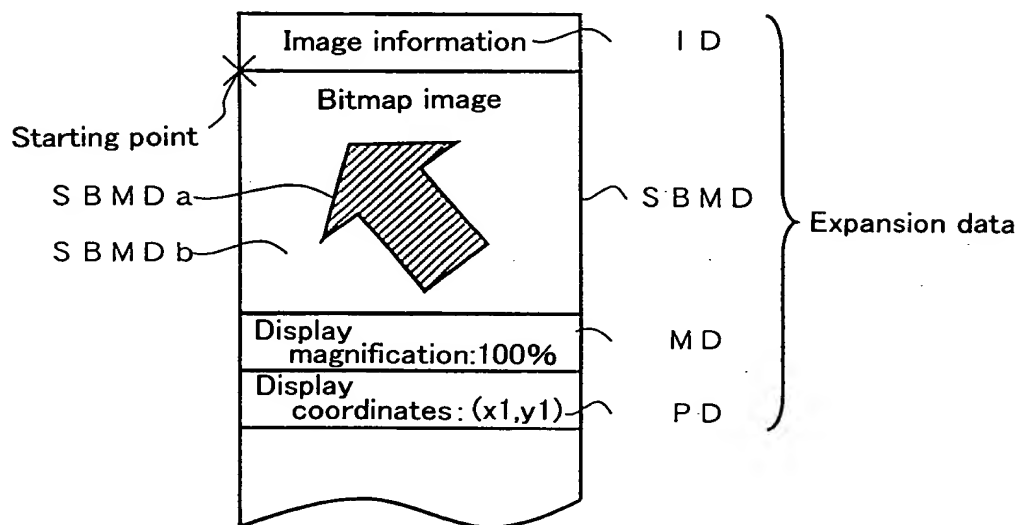


Fig.21(c)

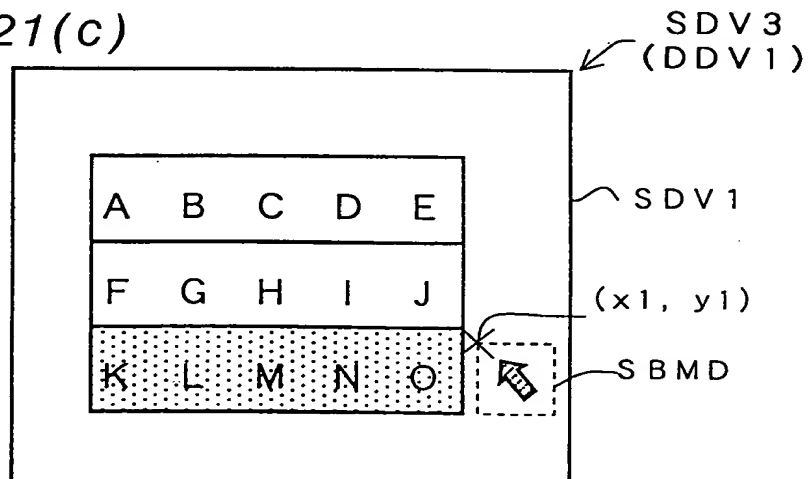


Fig. 22 (a)

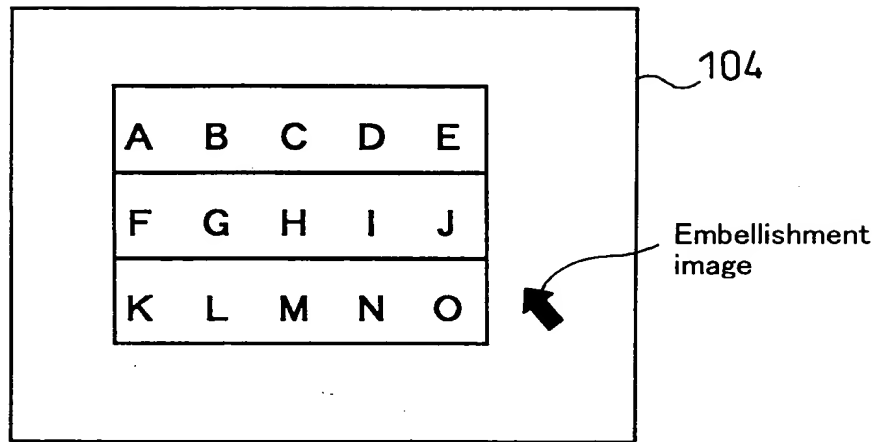


Fig. 22 (b)

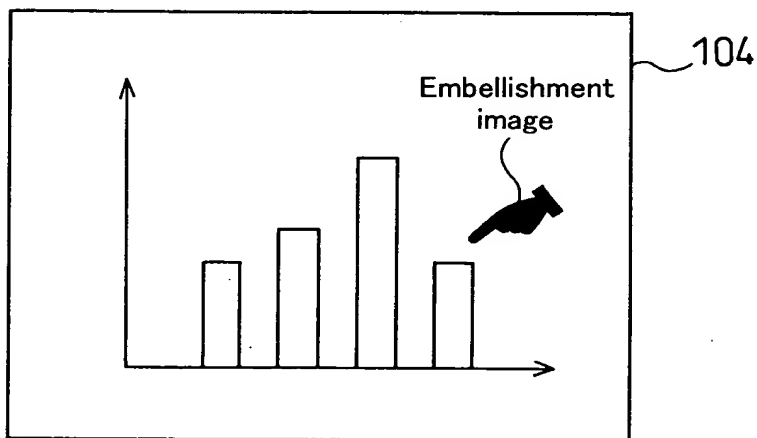


Fig. 22 (c)

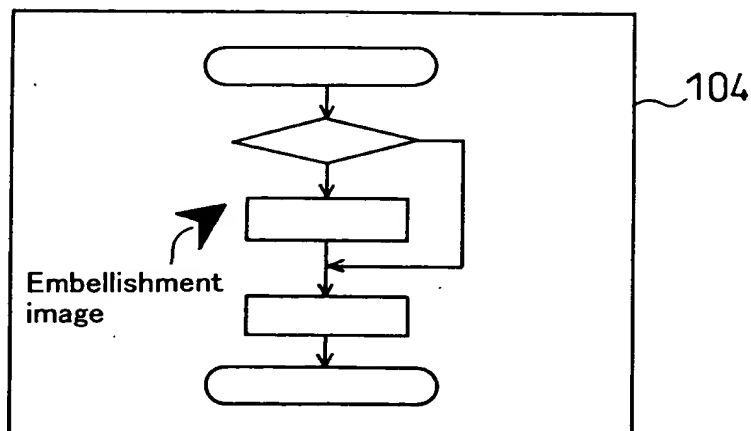


Fig. 23 (a)

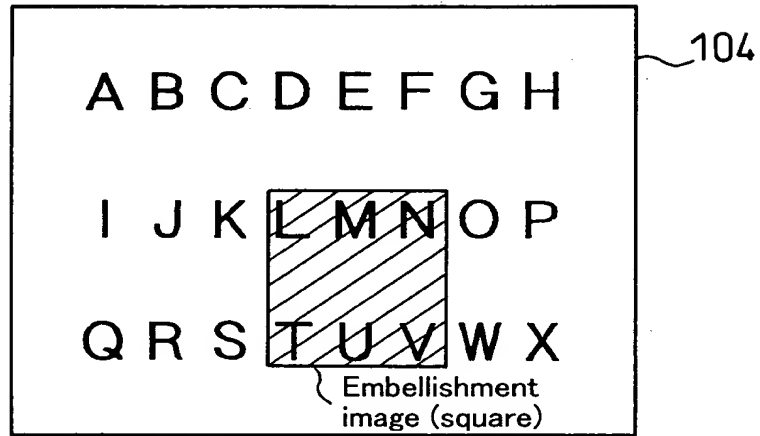


Fig. 23 (b)

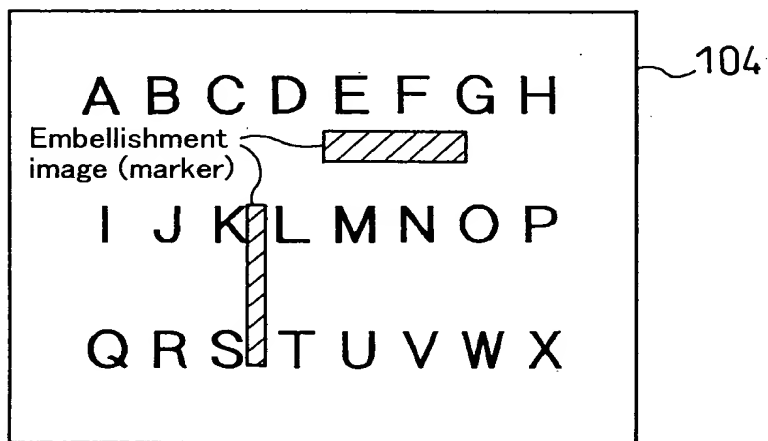


Fig. 23 (c)

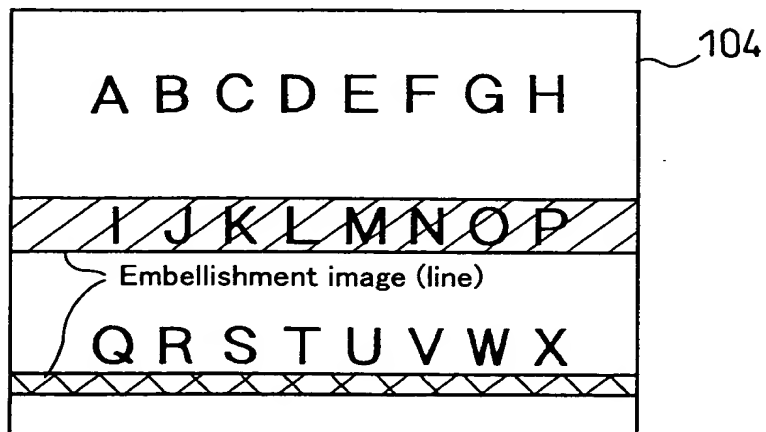


Fig. 27(a)

$$\begin{aligned} x_c &\geq x_1 \\ y_c &\geq y_1 \end{aligned}$$

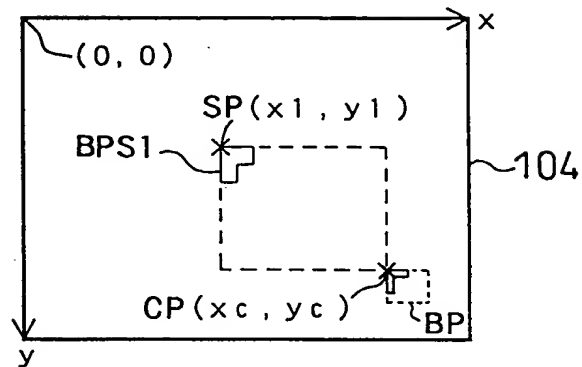


Fig. 27(b)

$$\begin{aligned} x_c &< x_1 \\ y_c &\geq y_1 \end{aligned}$$

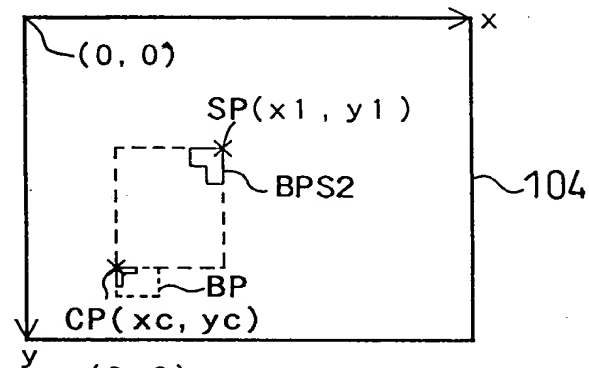


Fig. 27(c)

$$\begin{aligned} x_c &< x_1 \\ y_c &< y_1 \end{aligned}$$

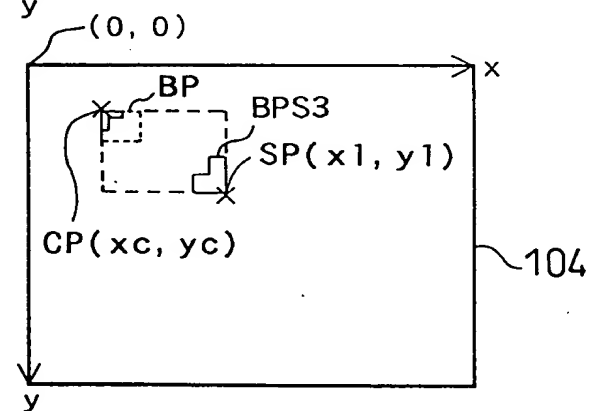


Fig. 27(d)

$$\begin{aligned} x_c &\geq x_1 \\ y_c &< y_1 \end{aligned}$$

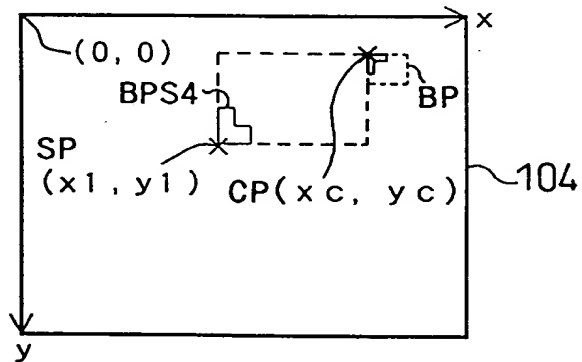


Fig. 28(a)

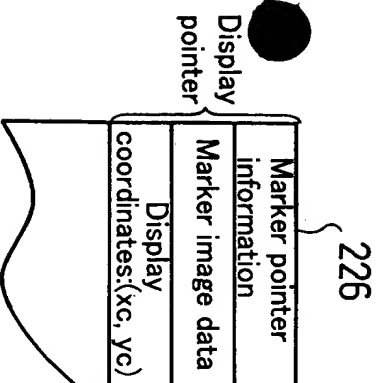


Fig. 28(b)

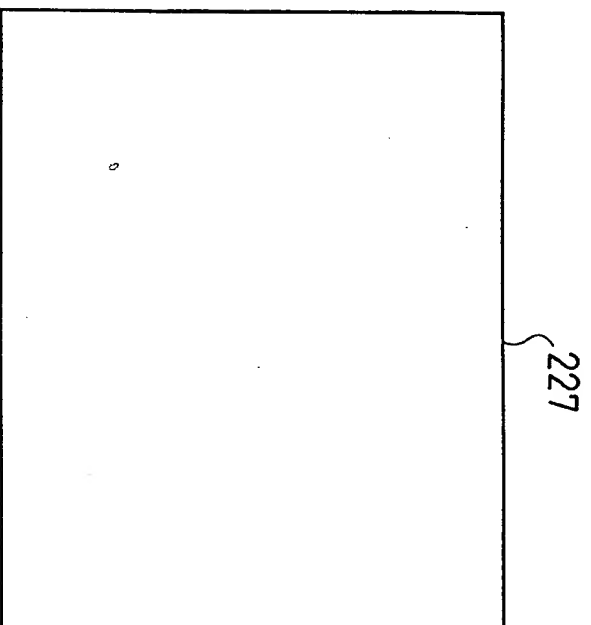


Fig. 28(c)

